Data Sheet for SDIO Slave Controller

iW-ASCD6-DS-01

R 1.0

16th Sep. '15

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APPROVAL

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Revision	Date	Change Description	Author
1.0	14th Nov '08	Initial Version	KT
1.1	26th Nov '08	Updated Modem Status Register Description	KT
1.2	13th Jan '09	Updated with detailed Block Diagram	KT
1.3	1st Apr '09	Updated register description	FA
1.4	24th Dec '11	Updated in new format	AS
1.5	27th Dec. '13	Added SDIO 3.0 support	AS
1.6	15th Sep. '15	No. of functions supported details updated	AS
1.7	16th Sep. '15	Improved Wishbone signals descriptions • Address bus width corrected • CTI,BTE signals included	RKB

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1 Introduction

1.1 Purpose

This document describes the Technical Specification of the SDIO Slave Controller. It includes the overall architectural description, detailed functional specifications and interface definitions for the SDIO Slave Controller.

1.2 Features

The following are the main features of the SDIO Slave Controller:

- Compliant with SD Physical Specification Version 3.00 and SDIO Specification Version 3.00.
- Supports 1-bit and 4bit SD modes.
- Supports SDIO Interrupt feature
- Supports all mandatory SDIO Commands/Response types
  - SPI Mode : CMD0, CMD5, CMD52, CMD53, CMD59
  - SD Mode: CMD0, CMD3, CMD5, CMD7, CMD52, CMD53.
- CRC7 checking/generation for Command/Response
- CRC16 checking/generation for Data transfer.
- Supports SDR12, SDR25, SDR50 and SDR104** Mode of operation.
- Supports only 1.8V or 3.3V SDIO Voltage. SDIO voltage switching is not supported.
- Data Transfer in Multi Byte and Multi Block mode using CMD53
- 8-bit Wishbone interface with constant burst, Wishbone Specification- B3 supported
- Function0 and Function1 supported
- SDIO only implementation, Combo card features are not supported
- Optional Code Storage Area(CSA) is not supported
- Suspend/Resume Features not supported
- DDR50 mode is not supported

*** IP Supports SDR50 and SDR104 mode. Please contact us to check the SDR50 and SDR104 mode support in target device.*

1.3 Acronyms and Abbreviations

Table 1: Acronyms & Abbreviations

Term	Meaning
CIA	Common I/O Area
CIS	Card Information Structure
CRC	Cyclic Redundancy Check
CSA	Code Storage Area
FIFO	First In First Out queue
FPGA	Field Programmable Gate Array
FSM	Finite State machine
GPIO	General purpose Input/Output
LSB	Least Significant Byte
MSB	Most Significant Byte
OCR	Operations Conditions Register
RAM	Random Access Memory
RCA	Relative Card Address
SDIO	Secure Digital Input Output
SPI	Serial Peripheral Interface

2 SDIO Slave Controller

2.1 Block Diagram

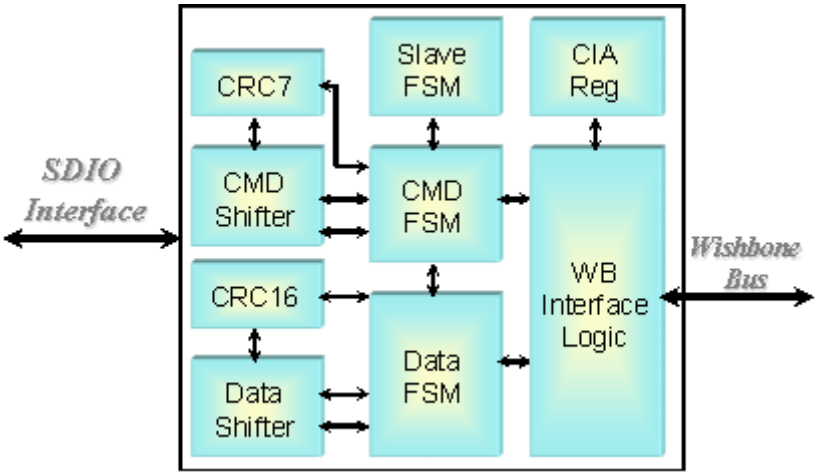

Figure 1: SDIO Slave Controller Block Diagram

2.2 Description

The main blocks in SDIO Slave Controller are

- **SDIO Slave**: This module has Logic that implements the SDIO Slave device. Here the Physical bus interface takes care of the Command and Data bus interface. This module supports CRC checking and generation for both Command and Data. SDIO Function0 registers and other registers are supported as per the SDIO specification. A Wishbone interface is supported to interface Device Function Area.
- **Watchdog timer**: This module is used to generate error signal to SDIO slave. The error signal will be generated when timeout count register reaches the maximum count. This error signal is used to terminate wishbone cycle when acknowledgement is not received from the wishbone slave.

2.3 I/O Signal Description

Table 2: System Interface IO Signal Description

Signal	I/O	Width	Description
SYS_RST_N_I	I	1	System Reset. Active Low Asynchronous reset input.
SYS_CLK_I	I	1	System Clock. Clock input to the SDIO Slave IP. This clock is also used as the wishbone interface clock output.

Table 3: SDIO Interface IO Signal Description

Signal	I/O	Width	Description
SD_CLK_I	I	1	SDIO Bus Clock input.
SD_CMD_IO	I/O	1	SDIO Command SDIO bi-directional line for command and response token.
SD_DAT_IO[3:0]	I/O	4	SDIO Data SDIO bi-directional lines for data read and write. SD_DAT_IO[1] line is also used by card to interrupt the host.

Table 4: Wishbone Interface IO Signal Description

Signal	I/O	Width	Description
WB_CLK_O	O	1	Wishbone Bus clock The clock output coordinates all activities for the wishbone interface logic. The clock output is same as the system clock input to the IP : SYS_CLK_I
WB_RST_O	O	1	Wishbone bus Reset Active high reset output
WB_ADDR_O[16:0]	O	17	Wishbone bus Address It is used to pass a binary address.

Signal	I/O	Width	Description
WB_DATA_I[7:0]	I	8	Wishbone bus data It is used to pass data for read operations
WB_DATA_O[7:0]	O	8	Wishbone bus data It is used to pass data for write operations
WB_WE_O	O	1	Wishbone Write Enable The active high write enable input indicates whether the current wishbone bus cycle is a READ or WRITE cycle. The signal is negated during READ cycles, and is asserted during WRITE cycles.
WB_STB_O	O	1	Wishbone Strobe This output is asserted, when a SLAVE is selected. A SLAVE will respond to other WISHBONE signals only when this is asserted.
WB_SEL_O	O	1	Wishbone Select. This output indicates where valid data is expected on the [wb_data_i] signal array during READ cycles, and where it is placed on the [wb_data_o] signal array during WRITE cycles. The array boundaries are determined by the granularity of a port. Since in the current implementation data port width is 8bit, this signal is 1bit.
WB_CYC_O	O	1	Wishbone Cycle This output is asserted to indicate that a valid bus cycle is in progress. The signal is asserted for the duration of complete bus cycle.

<table>
<tr><th>Signal</th><th>I/O</th><th>Width</th><th>Description</th></tr>
<tr><td>WB_CTI_O[2:0]</td><td>O</td><td>3</td><td>Wishbone Cycle type identifier
The CTI output signal provides information about the current cycle.
<table>
<tr><td>CTI[2:0]</td><td>Description</td></tr>
<tr><td>‘000’</td><td>Classic Cycle</td></tr>
<tr><td>‘001’</td><td>Constant address burst cycle</td></tr>
<tr><td>‘010’</td><td>Incrementing burst cycle</td></tr>
<tr><td>‘011’</td><td>Reserved</td></tr>
<tr><td>‘100’</td><td>Reserved</td></tr>
<tr><td>‘101’</td><td>Reserved</td></tr>
<tr><td>‘110’</td><td>Reserved</td></tr>
<tr><td>‘111’</td><td>End-of-Burst</td></tr>
</table></td></tr>
<tr><td>WB_BTE_O[1:0]</td><td>O</td><td>2</td><td>Wishbone Burst Type Extension
The BTE output signal provides information about the current burst. This information is related incremental burst.
<table>
<tr><td>BTE[1:0]</td><td>Description</td></tr>
<tr><td>‘00’</td><td>Linear burst</td></tr>
<tr><td>‘01’</td><td>4-bear wrap burst</td></tr>
<tr><td>‘10’</td><td>8-bear wrap burst</td></tr>
<tr><td>‘11’</td><td>16-beat wrap burst</td></tr>
</table>
* Currently IP core supports only Linear Burst mode, i.e., WB_BTE_O[1:0] hardcoded to ‘00’</td></tr>
<tr><td>FN1_INTR_I</td><td>I</td><td>1</td><td>User Function interrupt
This input indicates user function interrupt</td></tr>
<tr><td>WB_ACK_I</td><td>I</td><td>1</td><td>Wishbone Acknowledge
The active high input when asserted, indicates the termination of a normal bus cycle.</td></tr>
</table>

3 Timing Waveforms

3.1 SDIO Interface

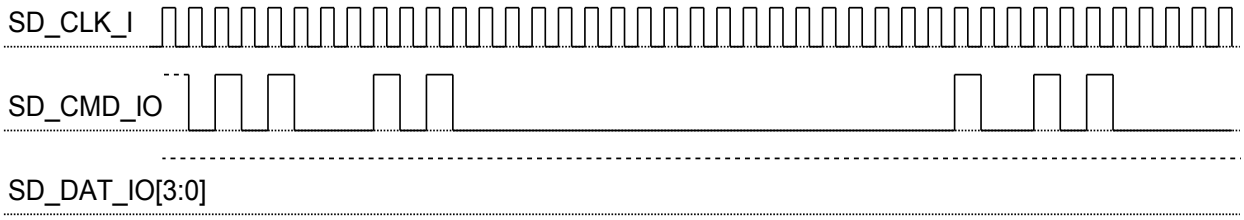

Figure 2: Command Write

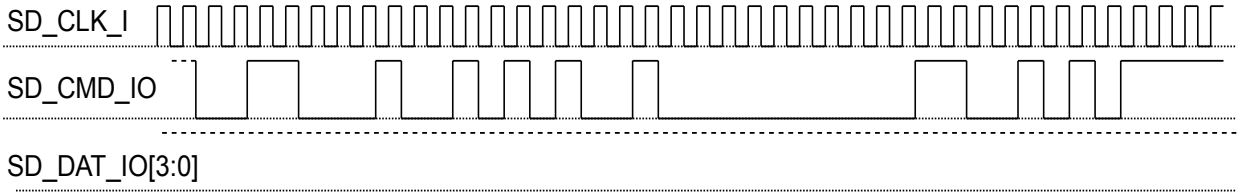

Figure 3: Response Read

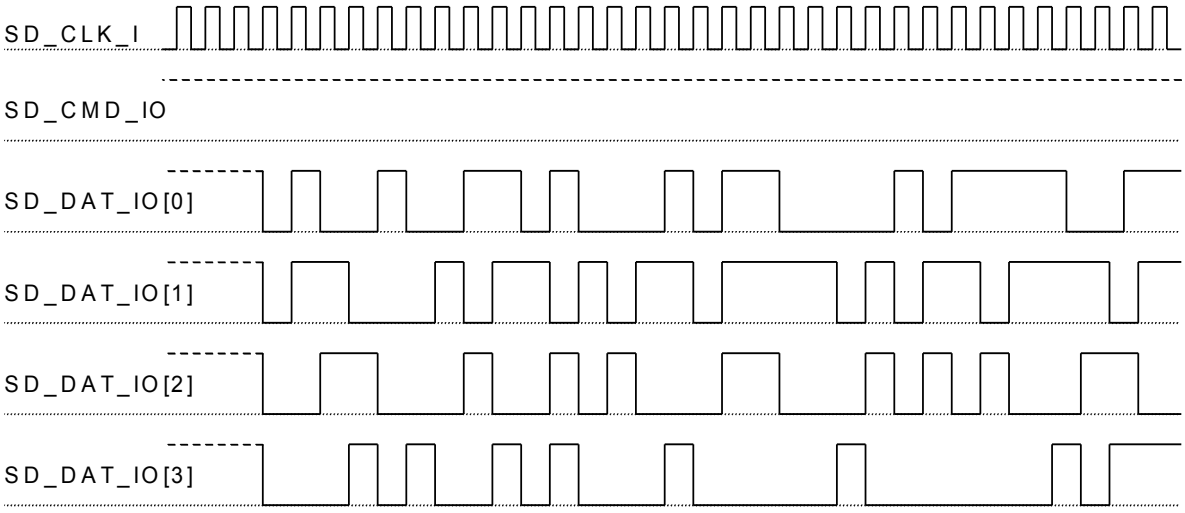

Figure 4: Data Write 4-bit mode (Data Transfer)

3.2 Wishbone Interface

3.2.1 Classic Cycle

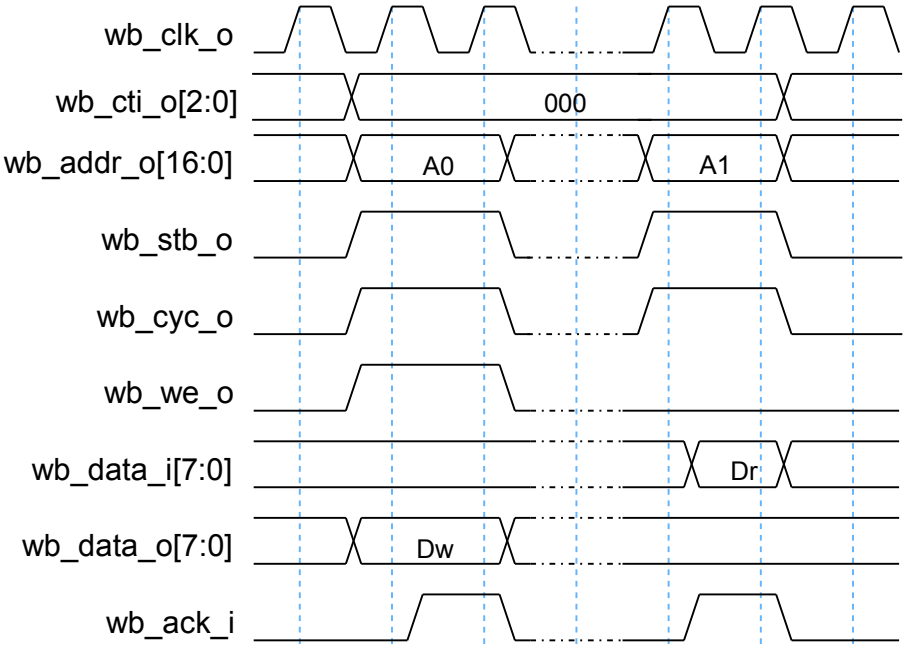

Figure 5: Wishbone Interface Classic Cycle Read/Write Timing Diagram

3.2.2 Burst Write Cycle

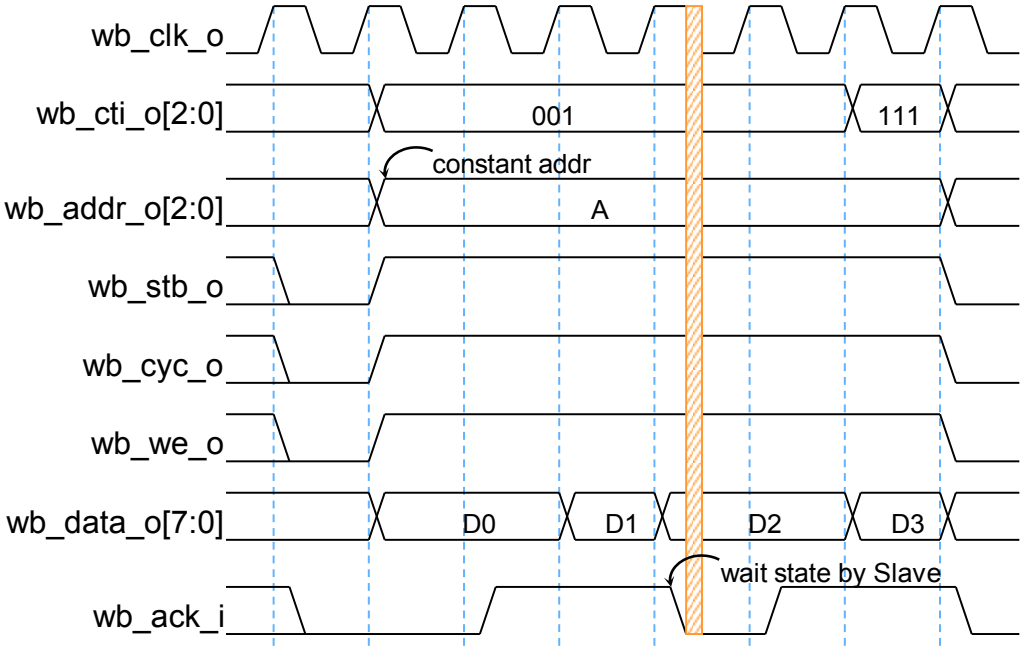

Figure 6: Wishbone Interface Burst Write Timing Diagram

3.2.3 Burst Read Cycle

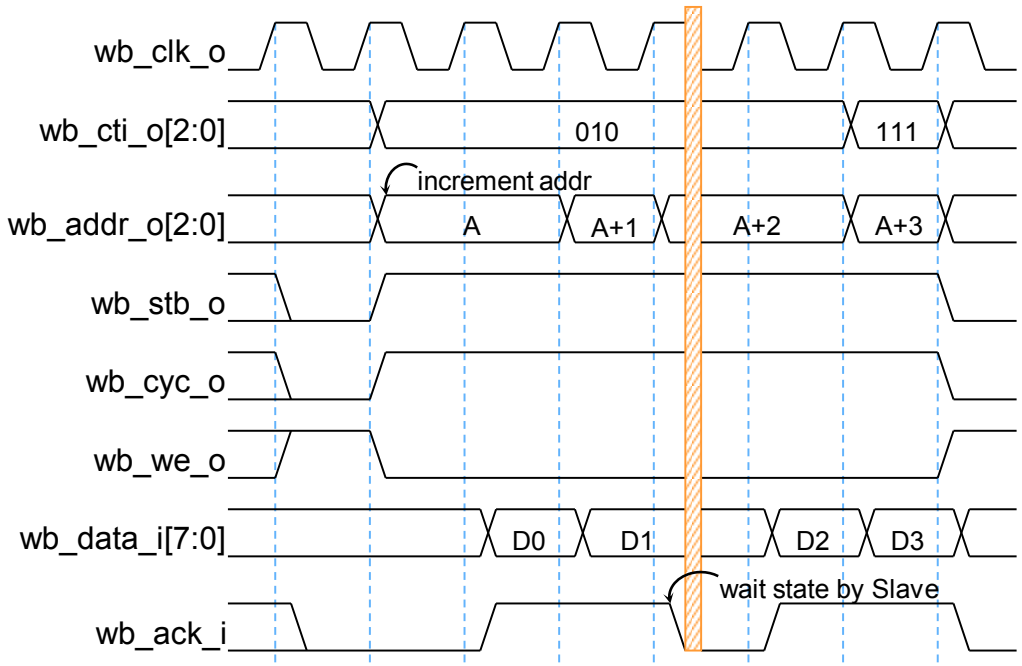

Figure 7: Wishbone Interface Burst Read Timing Diagram

4 Implementation Results

The table below shows the utilization summary from the implementation of SDIO Slave Core for FPGA devices.

Device Utilization Summary for Actel ProASIC3

Logic Utilization	Used
Number of Core SEQ	1081
Number of Core COMB	2280
RAM/FIFO	4
Number of IOs	46

Device Utilization Summary for Xilinx Spartan6

Logic Utilization	Used
Number of Slice Registers	1041
Number of Slice LUTs	1134
Number of RAMB8BWER	4
Number of IOs	46

Device Utilization Summary for Altera Cyclone IV E

Logic Utilization	Used
Number of Logic Elements combinational	1256
Number of Logic Elements registers	1036
Total Memory bits	2048
Number of Pins	46

Device Utilization Summary for Lattice XP2

Logic Utilization	Used
Number of Slice Registers	1090
Number of Slice LUTs	1550
Number of Block RAM	4
Number of PIO	46